An MMIC Amplifier for Automatic Level Control Applications

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ABSTRACT

An automatic gain control amplifier for automatically-leveled output power, broadband, swept frequency applications to 3GHz has been developed. Consisting of a variable π attenuator, four additive-gain amplifier stages, a temperature compensated peak detector and an output buffer, the amplifier features a maximum leveled gain of 22dB, a gain control range of 25dB, good input and output matches to 50Ω and suppressed 2nd harmonic distortion. It operates with ±6V power supplies and dissipates approximately 800mW.

AMPLIFIER OVERVIEW

Figure 1 depicts a functional block diagram of the amplifier. Those elements within the dashed box are integrated on the GaAs MMIC which was fabricated in a depletion mode MESFET process with a nominal pinch-off voltage of -2.1V(1).

At the input is a simple π attenuator consisting of two shunt resistors and a series FET. It provides a 25dB range of attenuation, is regulated by a single control voltage, and has a worst case return loss of 12dB. The attenuator is located at the input of the amplifier, where the signal is smallest, to minimize the distortion it introduces.

The signal from the attenuator is capacitively coupled to four additive-gain amplifiers.(2) Each stage has about 5dB of voltage gain when driving the input of a similar stage.

The output buffer provides constant voltage gain and a good match to 50Ω over the entire band (worst case return loss of 15 dB) so that the incident power to an external load is held constant. A logical extension of the additive amplifier, its push-pull operation provides suppression of 2nd harmonic distortion.

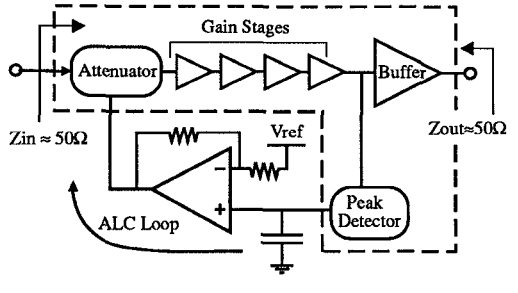

Fig. 1. Functional block diagram of the MMIC chip (inside dashed lines), being used to level output power against variations in input power.

A voltage peak detector located after the fourth gain stage, but before the output buffer, generates a signal which, when used to control an external feedback loop, allows voltage loop leveling. Hence, the output buffer delivers constant incident power to its load. If the detector were located at the output, the detected signal would depend on the load.

ATTENUATOR DESIGN AND PERFORMANCE

The attenuator topology is depicted in figure 2a. Consisting of one FET and two 60Ω fixed resistors, its virtues are that only one control voltage is needed and that it has an attenuation range of 25dB. Figure 2b depicts measured attenuation as a function of control voltage.

The attenuator also presents a reasonably good match to 50Ω. Figure 2c depicts measured S11 data of the attenuator for several values of the control voltage. The worst case match corresponds to a VSWR of about 1.7:1. Note that as attenuation

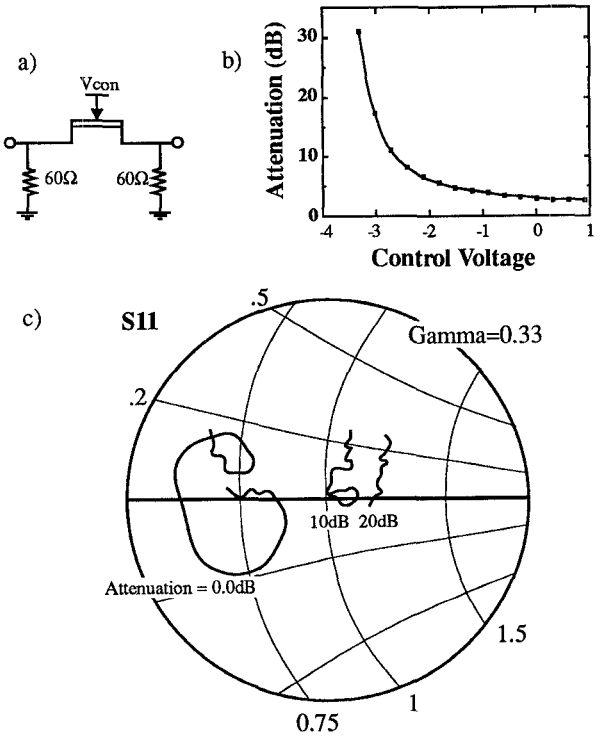

Fig. 2. a) One-control-terminal attenuator. b) Measured attenuation versus control voltage. c) Input reflection coefficient from 0.1 to 10 GHz for three values of attenuation.

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increases (more negative control voltages) the input match improves significantly. While attenuators with two or three active elements[3] offer better matches, they require two control voltages and are consequently more difficult to operate. In the present design, ease of operation was chosen over better input matching.

ADDITIVE-GAIN AMPLIFIER DESIGN

Four capacitively coupled additive-gain amplifiers similar to that reported in (2) are used as voltage gain cells. Figure 3a depicts the schematic of the cell. Flat frequency response is maintained by resonating each cell's capacitive load with the synthetic inductor consisting of Q2 and R1. The inverted signal at node A is peaked by the synthetic inductor and added to the signal inverted by Q3 through the source follower Q4. In designing the gain cells, gain and bandwidth were optimized to achieve the simulated response shown in figure 3b. The performance of the cell is comparable to that of other amplifier stages manufactured with the same process.[4][5]

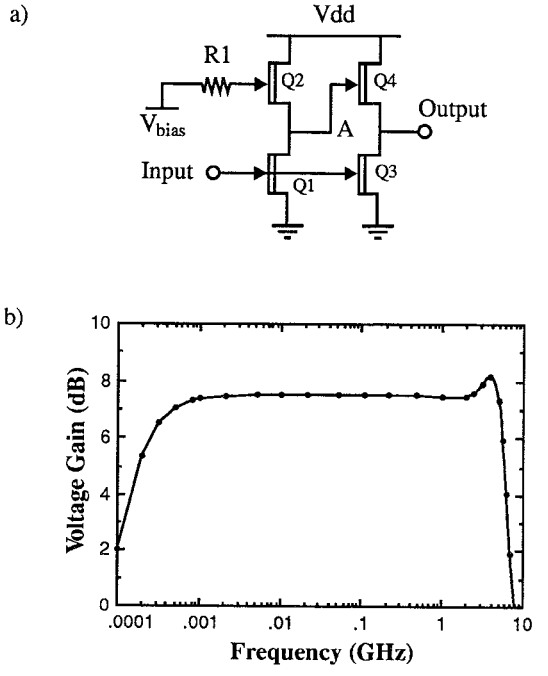

Fig. 3. a) The additive gain amplifier cell (similar to ref. [2]). b) Simulated frequency response of voltage gain for this cell driving a similar cell's input capacitance.

OUTPUT BUFFER DESIGN AND PERFORMANCE

The output buffer is designed to match to 50Ω and to minimize the 2nd harmonic. Figure 4a shows the two output FETs and demonstrates how 2nd harmonic distortion is reduced. To minimize the amplitude of the 2nd harmonic, the gate-to-source voltages of Q1 and Q2 should have the same amplitude but should be 180° out of phase. If this is the case, then the fundamental signals from both FETs will add whereas the 2nd harmonic signals will be equal in magnitude, but 180° out of phase and cancel. Expressing the desired equality of V_{gs} of the two FETs mathematically yields the result

$$\frac{V_{g2}}{V_{g1}} = \frac{1 + A_1}{1 - A_2}$$

where A_1 and A_2 are the gains of the inverting FET (Q1) and the source follower (Q2) respectively, and V_{g1} and V_{g2} are as shown in figure 4a.

The design approach, then, is to first choose the size of the output FETs such that their parallel output impedance is 50Ω, to determine the two gains A_1 and A_2, and then to design an inverting amplifier whose gain is given by the ratio of equation 1. As shown in figure 4b, the predicted gains A_1 and A_2 of the output FETs used in the present design were such that this ratio was 2.46 yielding a gain of 1.46 (3.3dB) for the output buffer. The inverting amplifier which supplies the signal to the gate of Q2 consists of FETs Q3 - Q8 in figure 4b. Resistor R1 and FET Q4 compose a synthetic inductor for peaking.

Because the signal V_{g2} of figure 4a will be delayed by the inverting amplifier relative to the signal V_{g1}, the signals will not be exactly 180° out of phase, and some 2nd harmonic distortion will occur. However, as shown in figure 5a, the 2nd harmonic is indeed suppressed. The fundamental for this measurement is at 300Mhz and the amplifier is operating open loop. For comparison, the arrow at 10 dBm output power in figure 5a indicates the 2nd harmonic magnitude corresponding to 10 dBm fundamental output (300Mhz) for a similar amplifier with a single, common source output transistor[2].

In testing the amplifier, it was discovered that a minimum in the 2nd harmonic occured as the negative supply voltage was varied. This minimum typically occured within a volt of the nominal -6 volt negative supply and reflects process variation of the transistor characteristics. Figure 5b depicts typical 2nd harmonic and fundamental output powers as the negative supply is varied. This data was taken with -10dBm input power. Note that at the null, corresponding to -6V, the second harmonic is 46dBm below the fundamental.

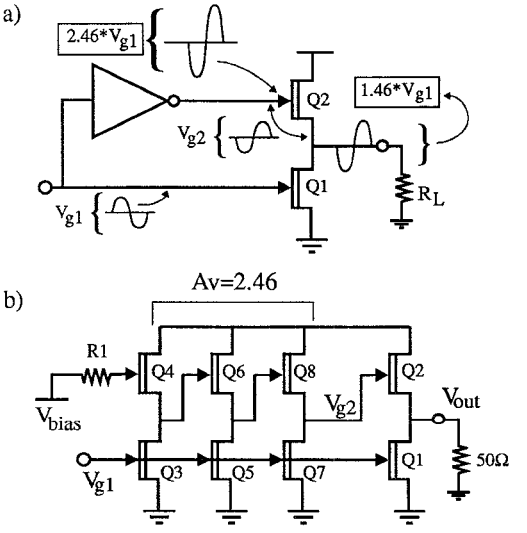

Fig.4. A push-pull output buffer with 50Ω output impedance which reduces second harmonic distortion can be constructed as shown in (a) using the inverting amplifier and two output FETs. The buffer schematic is shown in (b).

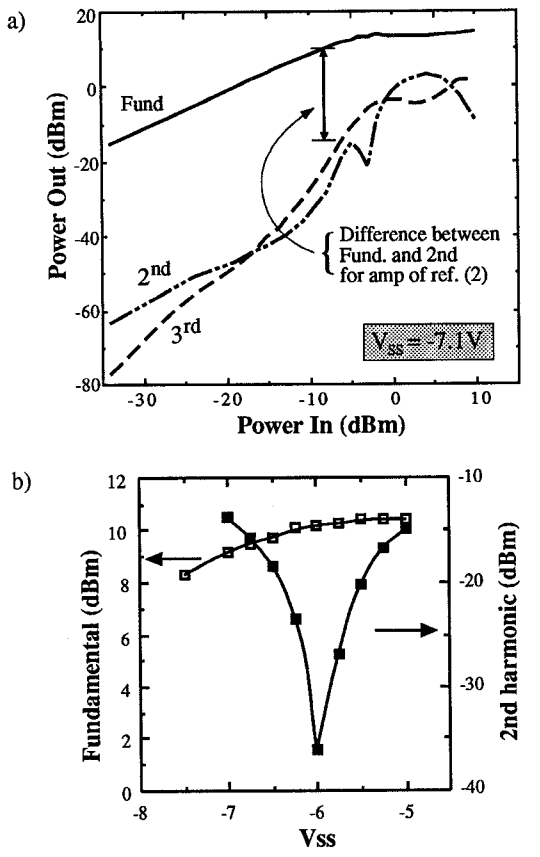

Fig. 5. a) Harmonic distortion versus power in. An improvement over the single FET output buffer of ref.[2] is achieved. b) Bias (Vss) dependence of second harmonic distortion. Data for figures a and b taken from different devices.

PEAK DETECTOR DESIGN

The output of the fourth gain stage is capacitively coupled to a balanced diode peak detector. It detects voltage before the output buffer, and hence, when an external feedback loop is employed, it levels voltage. Because the diode area is small, it presents a large reactive impedance to the signal at the output of the gain stage. Furthermore, for large amplitude signals, since the diode conducts for only a small portion of the signal cycle, it presents a large real dynamic impedance as well. Thus, the signal is not loaded significantly by the detector.

AMPLIFIER PERFORMANCE

The measured output match to 50Ω from 0.1 to 10 GHz is shown in figure 6a. The marker is at 3GHz where the return loss is 15dB. The VSWR is less than 1.5:1 over the band from 0.1 to 3GHz

Figure 6b depicts measured open loop gain versus frequency for several values of the attenuator control voltage. Because parasitic capacitances associated with the layout were not included in the simulation, the bandwidth of the amplifier is predictably lower than the simulated 4GHz. Also, actual gain was several decibels below the predicted gain. Testing below 100MHz has not been performed.

To test the amplifier closed loop, the simple 741 op amp feedback circuit shown in figure 1 was employed. V_{ref} and the input power were varied separately to test the leveling ability of the circuit. Figure 7 shows the closed loop gain versus frequency for a fixed V_{ref} of 0.315V and several values of the input power. Figure 7 can be understood by considering that when the input power is increased, the signal at the peak detector increases, causing the attenuator to attenuate the input signal; hence the network analyzer measures a lower S21. When each curve of figure 7 (except for the upper-most) is compared to the open loop response curves in figure 6b, it is seen that the closed loop amplifier does a good job of flattening the response to about 3.5GHz.

The performance of the amplifier compares favorably to that of reference (6) where a gain control stage based on reference (5) is used.

CONCLUSION

In summary, an MMIC amplifier for automatic loop leveling applications to 3GHz has been demonstrated. Integrating additive-gain amplifier stages, a low distortion output buffer, a peak detector and a variable attenuator on a single GaAs chip, the amplifier exhibits a maximum leveled gain of 22dB when the automatic level control loop is completed with an

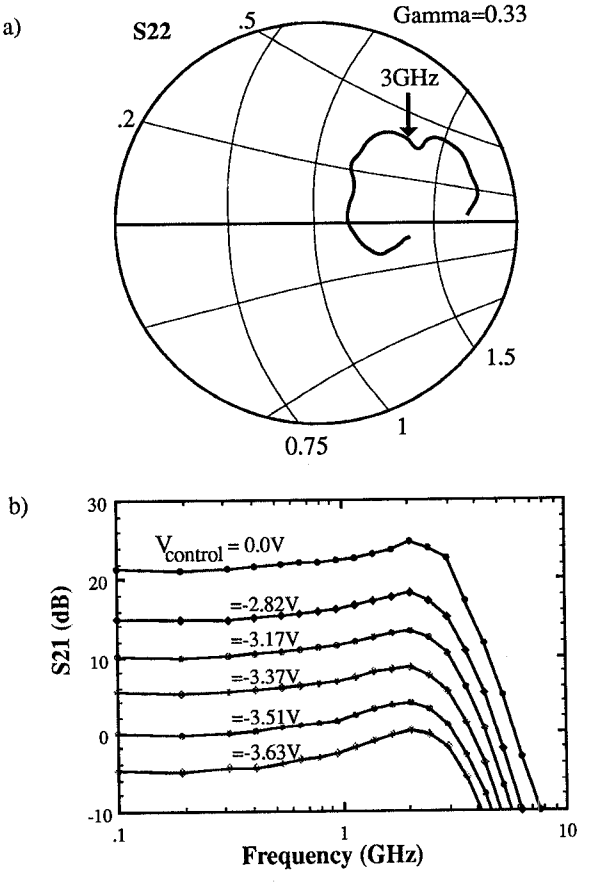

Fig. 6. a) Measured S22 of the amplifier. b) Measured S21 versus frequency for 5dB steps in input attenuation. S11 was shown in figure 2.

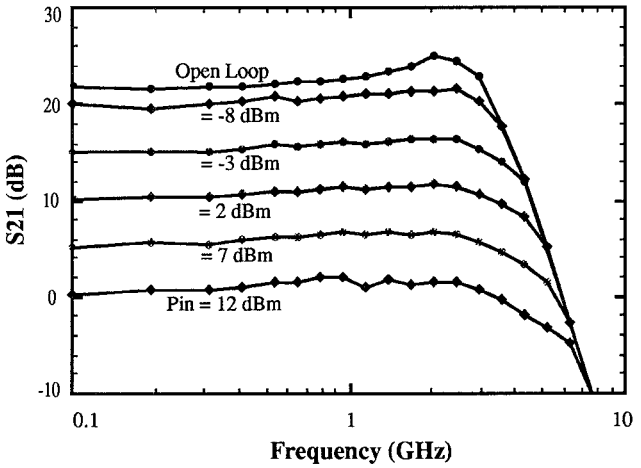

Fig. 7 Closed loop gain of amplifier in a level-control loop. Input power varied in 5dB steps while output power remains constant. (Irregularities in curves may be attributed to measurent technique.

op amp. The amplifier has a gain control range of 25dB, worst case input and output VSWRs of 1.7:1 and 1.5:1 respectively and dissipates approximately 800mW. Two possible uses of the amplifier would be in signal generation or in an amplitude modulation application with low modulation bandwidth.

ACKNOWLEDGEMENT

This work was supported in part by a grant from Hewlett-Packard Co., Microwave and Communications Group.

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